IN THE CLAIMS

Please cancel claims 1-7 and add the following new claims:

41. (New) A three dimensional memory array comprising:

a plurality of memory level pairs;

each memory level pair including a plurality of memory cells disposed on a first and second level;

the memory cells on the first level being coupled to first lines and common lines; and

the memory cells on the second level being coupled to second lines and the common lines.

42. (New) The array defined by claim 41, wherein each memory cell comprises a diode and a breached antifuse layer when programmed.

43. (New) The array defined by claim 42, wherein the first lines are disposed above the common lines and the second lines are disposed below the common lines.

44. (New) A memory disposed above a substrate comprising:

a plurality of memory levels organized as first alternate levels disposed between second alternate levels;

a plurality of two terminal memory cells incorporated into each of the levels;

one terminal of the cells in each of the first alternate levels and each of the second alternate levels being coupled to first lines shared by the cells in each pair of first and second alternate levels;

the other terminal of the cells in each of the first alternate levels being coupled to second lines; and

the other terminal of the cells in each of the second alternate levels being coupled to third lines.

45. (New) The memory defined by claim 44, wherein each cell comprises, when programmed, a diode and an antifuse layer.

46. (New) The memory defined by claim 45, wherein the diodes comprise an N- region and a P+ region.

47. (New) The memory defined by claim 46, wherein the N- regions in the diodes in at least one of the first and second alternate levels has a smaller cross-section than the P+ region.

48. (New) The memory defined by claim 45, wherein the antifuse layer comprises silicon dioxide.

49. (New) The memory defined by claim 47, wherein the antifuse layer comprises silicon dioxide.

50. (New) The memory defined by claim 46, wherein the diodes include polysilicon layers.

51. (New) The memory defined by claim 50, wherein the polysilicon layers include an N- layer and a P+ layer.

52. (New) The memory defined by claim 51, wherein the first, second, and third lines comprise a silicide.

53. (New) The memory defined by claim 52, wherein the silicide comprises titanium silicide.

54. (New) The memory defined by claim 53, wherein the shared first lines contact the P+ layers.

55. (New) A memory disposed above a substrate comprising:

a plurality of memory levels organized as first alternate levels disposed between second alternate levels;

a plurality of two terminal memory cells incorporated into each of the levels;

one terminal of the cells in each of the first alternate levels and each of the second alternate levels being coupled to first lines shared by the cells in each pair of first and second alternate levels;

the other terminal of the cells in each of the first alternate levels being coupled to second lines;

the other terminal of the cells in each of the second alternate levels being coupled to third lines; and

an oxide layer disposed between each of the pair of first and second alternate levels.

56. (New) The memory defined by claim 54, wherein each cell comprises, when programmed, a diode and a breached antifuse layer.

57. (New) The memory defined by claim 56, wherein at least some of the diodes comprise two regions, one having a smaller cross-section than the other.

58. (New) A memory disposed above a substrate comprising:

a plurality of memory levels, each level having a plurality of two terminal memory cells;

each of the memory cells comprising a diode and a breached antifuse layer, when programmed;

one terminal of the cells in first alternate levels and second alternate levels of the memory levels being coupled to first lines, shared by the cells;

the other terminal of the cells in the first alternate levels being coupled to second lines in each of the first alternate levels; and

the other terminal of the cells in the second alternate levels being coupled to third lines in each of the second levels,

such that cells in paired first and second alternate levels are coupled to shared first line and one of the second and third lines.

59. (New) The memory defined by claim 58, wherein at least some of the diodes have two regions one of which has a smaller cross-section than the other.

60. (New) In a three-dimensional memory array, two adjacent memory levels comprising:

a first plurality of parallel, spaced-apart rail-stacks;

a second plurality of parallel, spaced-apart rail-stacks perpendicular to the first rail stacks disposed above the first rail-stacks;

a third plurality of parallel, spaced-apart rail-stacks perpendicular to the second rail-stacks disposed above the second rail-stacks, the first, second, and third rail-stacks being of approximately the same height;

the first rail-stacks and a first portion of a second rail-stacks defining first cells in one of the two levels and the third rail-stacks and a second portion of the second rail-stacks defining second cells in the other level of the memory, and

the third rail-stacks including conductors shared by the first and second cells.

61. (New) The array of claim 60, wherein each cell comprises a diode and a breached antifuse layer, when programmed.

62. (New) The array of claim 61, wherein each diode includes a P+N- junction.

63. (New) The array of claim 62, wherein the antifuse layer of the cells comprises silicon dioxide.